In the Specification:

Please enter the following changes to the specification.

Please replace the BRIEF DESCRIPTION OF THE DRAWINGS section beginning at page 3, line 21, with the following:

FIG. 1 shows a schematic diagram of a typical SRAM binary content addressable memory ("CAM") cell;

FIG. 2 shows a schematic diagram of an exemplary 2k word by 64-bit CAM with four 16-bit segments;

FIG. 3 shows a schematic diagram for searchline pipeline logic and driver;

FIG. 4 shows a schematic block diagram for one word comparison, including "begin", "pipe" and "final" blocks used in a progressive search method for a segmented CAM;

FIG. 5 shows a table of some exemplary segmental search results for several words and the progressive search during different clocks;

FIG. 6 shows a timing diagram for compare operations with three continuous search data stacked together; and

FIG. 7 shows a table for power comparison between N-segmented architecture and non-segmented architecture for the same data width, where C is the capacitance for matchline or sinkline for one segment, and V is the supply voltage.

Please replace the paragraph beginning at page 4, line 23, with the following:

As shown in FIG. 2, a CAM is indicated generally by the reference numeral 20, and comprises searchline pipeline logic and driver 30, and 2k word by 64 bits cell array 40. The cell array further comprises four 16-bit wide segments of sub arrays, left edge, right edge, and gap blocks between segments. True and complimentary searchlines SL[0:15] and bSL[0:15] are delivered to segment 0, and SL[16:31] and bSL[16:31] to segment 1, SL[32:47] and bSL[32:47] to segment 2, and SL[48:63] and bSL[48:63] to segment 3. The left edge, right edge, and gaps also receive clock and precharge timing signal (bPRG). For wordline0, there are four segmented matchlines, i.e., matchline0_s0 for segment 0, matchline0_s1 for segment 1, matchline0_s2 for segment 2, and matchline0_s3 for segment 3. In addition, for wordline0, there are four segmented sinklines, i.e., matchline0_s0 for segment 0, matchline0_s1 for segment 1, matchline0_s2 for segment 2, and matchline0_s3 for segment 3. The "begin" block in the left edge of the cell array drives the matchlines and sinklines in segment 0. The "pipe" block in the gap area between two adjacent segments drives the matchlines and sinklines from one block to the next using a progressive search method. There is also a "final" block for receiving the matchlines and sinklines in the last segment.

Please replace the paragraph beginning at page 5, line 14, with the following:

Turning to FIG. 3, a searchline pipeline logic and driver block circuit is indicated generally by the reference numeral 30. Positive edge triggered D flip-flops are used to pipeline the 64 bit wide data into a CAM array with a synchronization clock. The first half of the clock cycle is the precharge phase where both SL and bSL are set to low (i.e., ground) by AND2 devices with signal bCLOCK as one of its inputs, to shut off the comparison in the CAM array. The second half of the clock cycle is the evaluation or comparison phase where the data to be searched are delivered on searchlines SLs and bSLs. SL[0:15] and bSL[0:15] are delayed from data[0:15] by one clock cycle, SL[16:31] and bSL[16:31] are delayed from data[16:31] by two clock cycles, SL[32:47] and bSL[32:47] are delayed from data[32:47] by three clock cycles, and finally, SL[48:63] and bSL[48:63] are delayed from data[48:63] by four clock cycles. Thus the comparison on each 16-bit segment of a word in the CAM array will be completed sequentially. A set of timing diagrams for SLs and bSLs is indicated generally by the reference numeral 600 of FIG. 6, as discussed below. The timing diagrams 600 include three continuous data sets for comparison purposes.

Please replace the paragraph beginning at page 6, line 3, with the following:

As shown in FIG. 4, a CAM array block is indicated generally by the reference numeral 40. Operation for one word is shown for illustration. As described above, each 64-bit word is compared in four 16-bit segments sequentially. In "begin" 41, matchline_s0 in segment 0 is precharged to high in a precharge phase, and sinkline_s0 in segment 0 is connected to low (ground). Therefore the comparison operation will always be performed for the first segment (i.e. segment 0) in the first clock cycle. If there is a mismatch for any word in segment 0, the matchline_s0 (which is the matchline for segment 0) corresponding to the mismatched word will be discharged to ground. Once there is a segmental mismatch for a particular wordline, the progressive search scheme will stop further comparison for that wordline in other segments since the word is already a mismatch regardless of the results in the other segments. In the meantime, the information of a first mismatch is passed along on the sinklines in the later segments by bringing those sinklines high.